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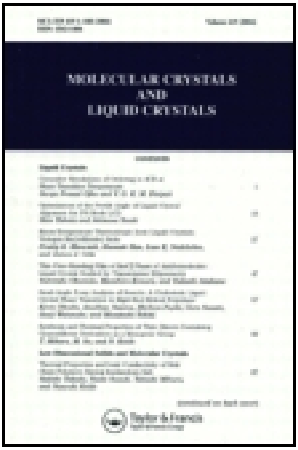

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Condensation and Annealing Effects of Polymer Gate Insulator on Organic Thin-Film Transistor Characteristics

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Condensation and Annealing Effects of Polymer Gate Insulator on Organic Thin-Film Transistor Characteristics

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Performances of organic thin-film transistors (TFTs) can be detrimentally affected by the state of gate dielectric layer. In this study, we report the condensation and annealing effects of a polymer gate dielectric layer. For the observations of the effect of condensation, the spin-coated polymer layers with various deposition conditions were fabricated and kept under low vacuum condition for several days. It is observed that the thickness of polymer layer and the electrical characteristics of organic TFTs vary with the condensation time, and the appropriate additional annealing process could stabilize the gate dielectric layer and even improve the device characteristics consequently.

Keywords: annealing; condensation; gate insulator; organic thin-film transistor

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INTRODUCTION

Recently, organic semiconductor devices, such as organic light-emitting diodes, organic thin film transistors (TFTs) and photodetectors, have been extensively investigated and steady progresses in device performances are continuously being obtained with ever increasing range of applications [1,2]. One of the most promising organic semiconductors is pentacene, mainly due to the high hole mobility of pentacene-based

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organic TFTs, and many researchers continue to develop high-performance pentacene-based organic TFTs, focusing on improving electrical device properties. And the polymeric dielectric gate materials, such as poly(4-vinylphenol) (PVP) and poly(methyl-methacrylate) (PMMA), have been reported for organic TFTs [3–5]. The choice of the appropriate gate dielectric material is an important criterion for a good organic TFT. Since organic TFTs are targeting a wide range of potentially inexpensive applications, alternative gate dielectrics and low-cost fabrication methods are of interest, including solution-processable polymer gate dielectrics which can be deposited by spin coating, spray coating, or printing, rather than by vacuum deposition [6,7]. However, there are still a number of problems when the polymer is used as the gate dielectric. One of the serious problems is in the cause of the physical and chemical stabilities of polymer films. In this work, the characteristic variations of organic TFTs with the PVP gate dielectric layer with polymer condensation time have been investigated.

EXPERIMENTAL DETAILS

The structures of fabricated organic TFT and PVP are shown in Figure 1. The inverted staggered structure was used for our devices. The active layer and metal electrodes were thermally evaporated through shadow masks on the PVP consequently. The pentacene, aluminum and gold were used as the active layer, gate electrode and source/drain electrodes respectively. The channel length and width of the fabricated organic TFTs were 100 μm and 5 mm, respectively. To investigate the stability of PVP insulating film, PVP was spin-coated with various weight percent, namely 4 wt%, 8 wt% and 10 wt%. Ethanol was used as the solvent for PVP, and the samples were prepared by coating the PVP layer at 2000 rpm, 3000 rpm, 4000 rpm and 5000 rpm respectively. The solvent was removed under the vacuum condition at 100°C during 1 hour (as-deposited PVP).

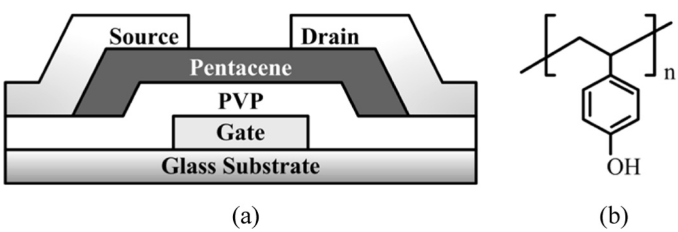

FIGURE 1 The structures of the fabricated organic TFT (a) and PVP molecule (b).

In order to observe the change of thickness with condensation time, the PVP film samples of various thicknesses were kept under the low vacuum circumstance.

RESULTS AND DISCUSSION

As shown in Figure 2, the PVP films got thinner with the time, but the PVP film deposited at the 2000 rpm shows no change in the thickness up to 5 days. In order to investigate the organic TFT characteristics relevant to the thickness variation of the PVP films, the devices were favricated with the PVP gate dielectric layers with various condensation or keeping time in the vacuum. The electrical characteristics of organic TFT with the PVP gate dielectric layer spin-coated at 4000 rpm with 8 wt% PVP solution in ethanol are shown in Figure 3. As expected, the saturation currents of organic TFTs with the PVP layers kept and condensed in the vacuum for 5 days were increased, which indicates that the gate capacitance increase was derived from the decreased thickness of the dielectric layer. The PVP film thickness decreases with the condensation time and the electrical characteristics of organic TFTs with the PVP layers also vary.

In order to eliminate this effect, the insulating layer was annealed for 1 hour at 180°C with 3 mtorr argon gas circumstance. The thickness of the annealed insulator decreased few nano-meters even with the 5-day

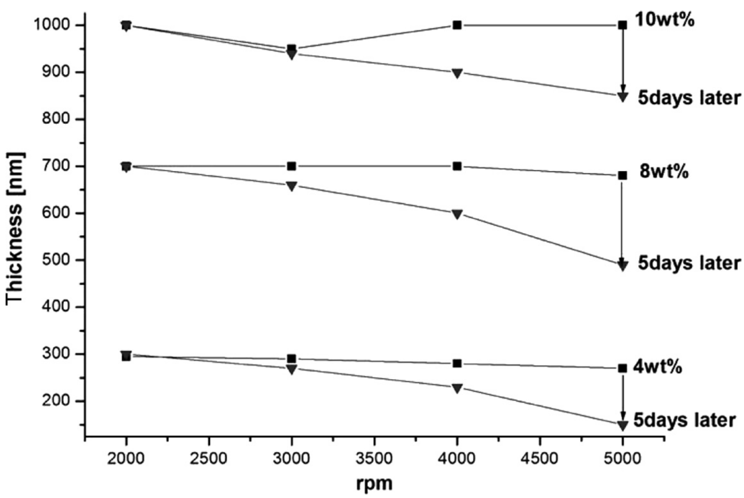

FIGURE 2 The thickness of PVP film chages with various conditions and condensation time.

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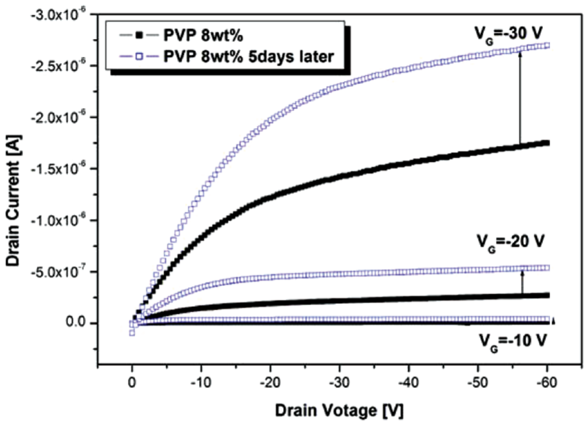
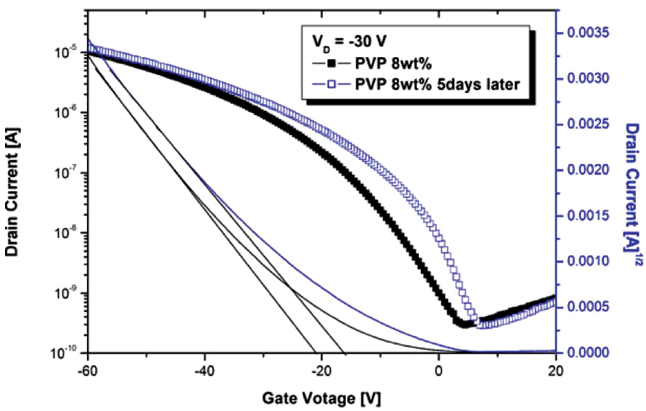


(a)



(b)

FIGURE 3 The electrical characteristic variation of organic TFT with the PVP gate insulator condensation.

condensation in the vacuum. And as shown in Figure 4, the electrical characteristics of organic TFT with the annealed insulator were substantially improved. The threshold voltage of the device with the annealed gate insulator was -9 V, which was decreased from -21 V for the device with the unannealed insulator, and the subthreshold slope was improved from 6.4 V/decade to 2.9 V/decade. Furthermore, the field-effect mobility was also increased from 0.08 cm^2/Vs to 0.41 cm^2/Vs.

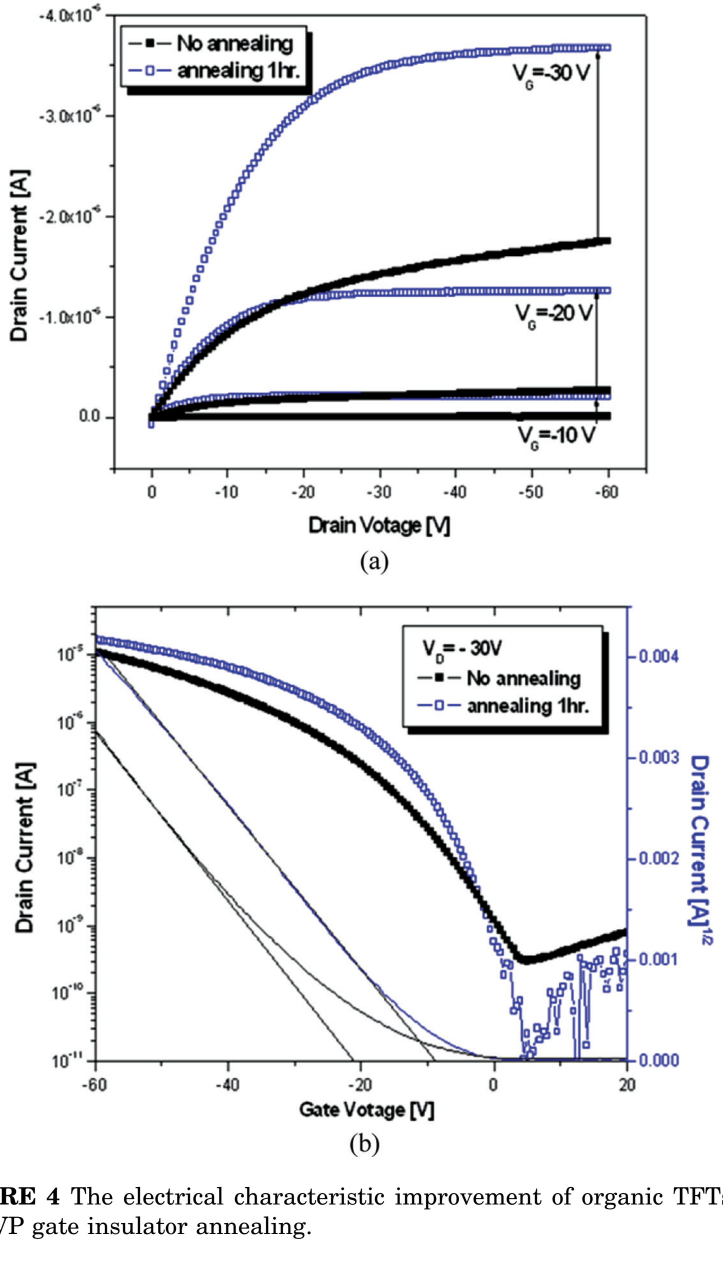


FIGURE 4 The electrical characteristic improvement of organic TFTs with the PVP gate insulator annealing.

The surface morphologies of the pentacene films deposited on different PVP insulators were studied using atomic force microscopy (AFM). All pentacene films were thermally evaporated on the PVP

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layers formed with various coating and annealing conditions. The thickness of the pentacene layers was 30 nm, and the deposition rate was 0.5 Å/sec. Figure 5(a) shows the surface image of the pentacene film deposited on the as-deposited PVP layer, which exhibits polycrystalline features of the film. Figure 5(b) is the AFM image of the pentacene film on the annealed PVP film. Figures 5(c) and (d) are the AFM images of the pentacene films on the as-deposited and annealed PVP films spin-coated using 2-butalethanol as a solvent, respectively. The grain size of the pentacne film on the thermally annealed PVP layer is larger and more uniform than that on the as-deposited PVP layer, which may be attributed by the surface potential

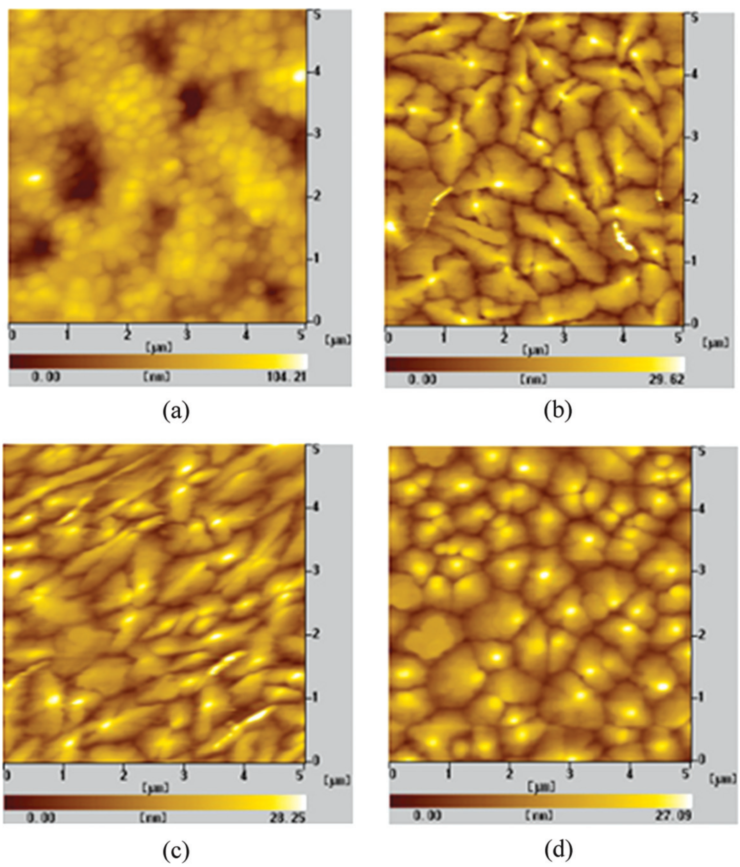

FIGURE 5 AFM images of pentacene films deposited onto as-deposit PVP (a), annealed PVP (b), as-deposit PVP dessolved in 2-butalethanol as a solvent (c), and annealed PVP dessolved in 2-butalethanol (d).

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change of the annealed PVP film. Molecular ordering also benefits from the smooth surface of the under-layer of the annealed PVP film [8]. This suggests that the condensation of PVP layer is deeply related to the processing condition of PVP layer and the concomitant morphology of pentacene film deposited on the underlaid PVP layer.

CONCLUSION

The pentacene-based organic TFTs with the PVP gate insulators have been investigated. The properties of pentacene films are closely correlated with those of the underlaid PVP gate dielectric layers. By additional thermal annealing of PVP dielectric layers, their thickness variation with the condensation time, which can occur in simply spin-coated and condensed PVP films, could be eliminated, and organic TFT operational characteristics as well as properties of pentacence films deposited on the annealed PVP layers were substantially improved. The optimized spin-coating and annealing recipe of the PVP film for reliable and high-performance organic TFTs could be suggested. It is also revealed that the PVP dielectric layer with the appropriately selected solvent for PVP may enhance the molecular ordering or crystallinity of the pentacene film deposited on that PVP dielectric layer, although high gate leakage current limited the fully optimized device performance. Most characteristic parameters of organic TFTs such as on/off current ratio, threshold voltage and carrier mobility are enhanced by optimizing the coating and annealing methods for the PVP gate insulator of organic TFTs.

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